IT IS CLAIMED:

1. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a plurality of circuit stress time values;

supplying aging model information on selected ones of the components;

simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective aging model information and respective relative component degradation parameter at the supplied circuit stress time values.

2. The method of claim 1, wherein said degradation of the circuit is due to hot-carrier effects.

3. The method of claim 1, wherein the simulating is performed using a SPICE type circuit simulator.

4. The method of claim 1, wherein the simulating is performed using a timing simulation type circuit simulator.

5. The method of claim 1, wherein the aging model information on the selected ones of the components is derived from electrical test data.

6. The method of claim 1, wherein said simulating the behavior of the fresh circuit determines the waveforms at the nodes to which the selected ones of the components are connected relative to an input waveform.

7. The method of claim 1, wherein determining the degraded operation of the circuit comprises determining the circuit's speed at the supplied circuit age parameters.

8. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit, wherein the circuit includes a plurality of distinct sets of components;

supplying an independent performance criterion for each set of said plurality of distinct sets of components;

supplying a circuit stress time value;

supplying aging model information on selected components from each of said sets of components;

simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time, wherein each of the selected components' relative degradation parameter is determined using the respective performance criteria of the set to which the selected component belongs; and

determining the degraded operation of the circuit by simulating the operation of the circuit with each of the specified components using the respective aging model information and respective relative component degradation parameter at the supplied circuit stress time value.

9. The method of claim 8, wherein the distinct sets of components each form different functional blocks.

10. The method of claim 8, wherein a first of said sets of components is an analog block and a second of said sets of components is a digital block.

11. The method of claim 10, wherein the performance criterion of the first set is transconductance and the performance criterion of the second set is drain to source current.

12. The method of claim 8, wherein the distinct sets of components consist of different device types.

13. The method of claim 12, wherein a first of said different device types is an NMOS and a second of said different device types is a PMOS.

14. The method of claim 13, wherein the PMOS performance criterion is leakage current.

15. The method of claim 13, wherein the NMOS performance criterion is driving capability.

16. The method of claim 12, wherein a first of said different device types is a MOSFET and a second of said different device types is a bipolar junction transistor.

17. The method of claim 16, wherein the bipolar junction transistor performance criterion is leakage current.

18. The method of claim 8, wherein the distinct sets of components employ different models for simulating the same device type.

19. The method of claim 8, wherein the distinct sets of components consist of the same device type.

20. The method of claim 8, wherein the distinct sets of components form functional blocks performing the same function.

21. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

supplying aging model information on a first set of selected components of the circuit;

simulating the behavior of the fresh circuit to determine for each of the first selected set of components a component degradation parameter relative to circuit stress time;

specifying the degradation level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct; and

determining the degraded operation of the circuit by simulating the operation of the circuit with each of the first set of specified components using the respective aging model information and respective relative component degradation parameter at the supplied circuit stress time value and with each of the second set of specified components using the respective specified degradation level.

22. The method of claim 21, wherein the first and second sets of components each form different functional blocks.

23. The method of claim 21, wherein the second set of components form a digital block.

24. The method of claim 23, wherein the specified degradation level is expressed in terms of drain to source current degradation.

25. The method of claim 21, wherein the second set of components is an analog block.

26. The method of claim 25, wherein the specified degradation level is expressed in terms transconductance degradation

27. The method of claim 21, wherein the first and second sets of components each consist of different device types.

28. The method of claim 27, wherein the second set of components consists of PMOS transistors.

29. The method of claim 28, wherein the specified degradation level is expressed in terms of leakage current degradation.

30. The method of claim 27, wherein the second set of components consists of NMOS transistors.

31. The method of claim 30, wherein the specified degradation level is expressed in terms of driving capability degradation.

32. The method of claim 27, wherein the second set of components consists of bipolar junction transistors.

33. The method of claim 32, wherein the specified degradation level is expressed in terms of leakage current degradation.

34. The method of claim 21, wherein the first and second sets of components employ different models for simulating the same device type.

35. The method of claim 21, wherein the first and second sets of components each consist of the same device type.

36. The method of claim 21, wherein the first and second sets of components form functional blocks performing the same function.

37. The method of claim 21, wherein the degradation level of the second set of selected components is specified as a relative component degradation parameter with respect to the component degradation parameter of the first set of components.

38. The method of claim 21, wherein the degradation level of the second set of selected components is expressed in terms of age.

39. The method of claim 21, wherein the degradation level of the second set of selected components is expressed in terms of lifetime.

40. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a plurality of circuit stress time values;

providing a device degradation table;

determining for selected ones of the components a component degradation parameter relative to circuit stress time from the device degradation table; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective relative component degradation parameter at the supplied circuit stress time values.

41. The method of claim 40, wherein the device degradation table is expressed in terms of one or more intermediate quantities.

42. The method of claim 41, wherein the device degradation table is time independent.

43. The method of claim 42, wherein the device degradation table is an age rate table.

44. The method of claim 41, wherein the device degradation table is a function of bias voltages.

45. The method of claim 40, wherein said providing a device degradation table comprises:

supplying aging model information on selected ones of the components;

simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation parameter relative to circuit age; and

storing an intermediate quantity derived from the relative component degradation parameters as said device degradation table.

46. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

providing a device degradation table expressed in terms of device current;

determining for selected ones of the components a component degradation parameter relative to circuit stress time from the device degradation table; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective relative component degradation parameter at the supplied circuit stress time value.

47. The method of claim 46, wherein the device degradation table is expressed in terms of gate current.

48. The method of claim 46 wherein the device degradation table is expressed in terms of substrate current.

49. The method of claim 46, wherein the device degradation table is expressed in terms of the ratio of substrate current to drain to source current.

50. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

providing a device degradation table;

determining for selected ones of the components a component degradation parameter relative to circuit stress time from the device degradation table; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective relative component degradation parameter at the supplied circuit stress time value, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said providing a device degradation table is embedded in the circuit simulator.

51. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

supplying aging model information on selected ones of the components;

simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time;

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version, wherein the magnitude of the current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a distinct mechanism degradation parameter derived from the component degradation parameter; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time value.

52. The method of claim 51, wherein the selected components are MOSFETs.

53. The method of claim 52, wherein said degradation of the circuit is due to hot carrier effects.

54. The method of claim 52, wherein for each of said selected components more than one of said plurality of independent current sources are connected between the source and drain terminals of the non-aged version.

55. The method of claim 52, wherein said method further includes:

determining the magnitude of the respective current in each of the independent current sources, said determining comprising:

supplying a physical model of the current magnitude; and

establishing the values of the coefficients in the physical model from electrical test data.

56. The method of claim 52, wherein the degradation level of the selected components is expressed in terms of lifetime.

57. The method of claim 52, wherein the degradation level of the selected components is expressed in terms of age.

58. The method of claim 51, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said revising the netlist is embedded in the circuit simulator.

59. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

supplying aging model information on selected ones of the components;

simulating the behavior of the circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time, wherein said simulating the behavior is performed using a circuit simulator and includes incorporating the aging of the selected components by updating the models of said circuit simulator;

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of

independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version, wherein the magnitude of the current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a distinct mechanism degradation parameter derived from the component degradation parameter; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time value.

60. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

supplying aging model information on selected ones of the components;

simulating the behavior of the circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time, wherein said simulating the behavior is performed using a circuit simulator and includes incorporating the aging of the selected components by updating the models of said circuit simulator; and

determining the degraded operation of the circuit at the supplied stress time value by simulating the operation of the circuit with the each of the specified components using the respective aging model information and respective relative component degradation parameter at the supplied stress time value.

61. The method of claim 60, wherein the selected components are MOSFETs and said incorporating the aging of the selected components comprises including the time dependence of the drain to source current.

62. The method of claim 61, wherein said incorporating the aging of the selected components comprises including the time dependence of the substrate current.

63. The method of claim 61, wherein said incorporating the aging of the selected components comprises including the time dependence of the gate current.

64. The method of claim 60, wherein said simulating the behavior of the circuit to determine for each of the selected components a component degradation parameter relative to circuit age comprises:

simulating the behavior of the fresh circuit to determine for each of the selected components an intermediate component degradation parameter relative to circuit stress time;

determining the degraded operation of the circuit at an intermediate circuit stress time value by simulating the operation of the circuit with the each of the specified components using the respective aging model information and respective relative intermediate component degradation parameter at the intermediate circuit stress time value; and

simulating the behavior of the degraded circuit at the intermediate circuit stress time value to determine for each of the selected components a component degradation parameter relative to circuit age, wherein the intermediate circuit stress time value is less than the circuit stress time value.

65. The method of claim 60, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said incorporating the aging of the selected components by updating the models of said circuit simulator is embedded in the circuit simulator.

66. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

providing for selected ones of the components model cards containing a device degradation parameter;

supplying a circuit stress time value;

simulating the behavior of the fresh circuit to determine for each of the selected components a device degradation parameter value relative to stress time; and

determining the degraded operation of the circuit by simulating the operation of the circuit with each of the selected components' model cards using the

respective device degradation parameter corresponding to the supplied circuit stress time value.

67. The method of claim 66, wherein said simulating the operation of the circuit is performed by a circuit simulator comprising an engine and a model evaluation module, and wherein said component degradation parameter is determined in the model evaluation module.

68. The method of claim 66, wherein the device degradation parameter is an intermediate quantity.

69. The method of claim 66, wherein the device degradation parameter is device lifetime.

70. The method of claim 66, wherein the device degradation parameter is device age.

71. The method of claim 66, wherein the device degradation parameter is device degradation.

72. The method of claim 66, wherein the selected components model cards are implemented as a subcircuit.

73. The method of claim 66, wherein the model cards containing a device degradation parameter contain one or more device model parameters as functions of said device degradation parameter.

74. The method of claim 73, wherein the functions of said device degradation parameter are extracted from experimental data.

75. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a circuit stress time value;

supplying aging model information on selected ones of the components;

simulating the behavior of the fresh circuit to determine for each of the selected components a degradation level relative to circuit stress time;

quantizing each of said relative degradation levels to one of a plurality of discrete values; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective aging model information and respective quantized relative degradation level at the supplied circuit stress time value.

76. The method of claim 75, wherein said determining comprises:

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources corresponding to different mechanisms with distinct quantized relative degradation level connected between the terminals of the non-aged version, the magnitude of the respective quantized current in each of the current sources determined from the aging model information of component; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist, the independent current magnitudes derived form the respective aging model information and respective relative degradation level at the supplied circuit stress time value.

77. The method of claim 75, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said quantizing is embedded in the circuit simulator.

78. A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the circuit at the device level;

supplying a circuit stress time value;

supplying aging model information on selected ones of the devices of which the circuit is comprised;

simulating the behavior of the fresh circuit with a circuit simulator;

determining for each of the selected devices a degradation parameter relative to circuit stress time, wherein said determining is embedded in said circuit simulator and is model independent; and

simulating the degraded operation of the circuit with the specified components using their respective aging model information and respective relative device degradation parameter at the supplied circuit stress time value.

79. The method of claim 78, wherein said selected devices are MOSFETs.

80. The method of claim 78, further comprising:

quantizing each of said device degradation parameters to one of a plurality of discrete values, wherein said simulating the degraded operation is performed using the quantized device degradation parameters.

81. The method of claim 80, wherein said quantizing is embedded in the circuit simulator.

82. A system for a user to simulate the degraded operation of a circuit, comprising:

a circuit degradation simulator;

a user defined circuit simulator, wherein said user defined circuit simulator allows the user to input a user selected circuit simulator and user data comprising:

a netlist representation of the circuit; and

a circuit stress time value; and

an interface for connecting the user defined circuit simulator to the circuit degradation simulator, whereby the circuit degradation simulator determines the operation of the circuit at the circuit stress time value utilizing said netlist representation in the user selected circuit simulator.

83. The system of claim 82, wherein said user selected circuit simulator is a SPICE type simulator.

84. The system of claim 82, wherein said user selected circuit simulator is a timing simulator.

85. The system of claim 82, wherein said user data further comprises:

a user selected device age model, wherein the circuit degradation simulator utilizes said user selected auxiliary function in determining the operation of the circuit at the circuit stress time value.

86. The system of claim 82, wherein said user data further comprises:

a user device degradation model, wherein the circuit degradation simulator utilizes said user device degradation in determining the operation of the circuit at the circuit stress time value.

87. The system of claim 86, wherein said user data further comprises:

a user selected auxiliary function, wherein the circuit degradation simulator utilizes said user selected auxiliary function in determining the operation of the circuit at the circuit stress time value.

88. The system of claim 87, wherein intermediate results in determining the operation of the circuit at the device age parameter are exchanged between said user device degradation model and said user selected auxiliary function.

89. The system of claim 88, wherein said user selected auxiliary function is the substrate current.

90. The system of claim 88, wherein said user selected auxiliary function is the gate current.

91. A computer readable storage device embodying a program of instructions executable by a computer to perform the method of any one of claims 1, 8, 21, 46, 50, 51, 59, 60, 66, 75, and 78.

92. A method for transmitting a program of instructions executable by a computer to perform a process of simulating the degradation of a circuit, said method comprising:

causing the transmission to a client device a program of instructions, thereby enabling the client device to perform, by means of such program, the process of the method of any one of claims 1, 8, 21, 46, 50, 51, 59, 60, 66, 75, and 78.